REMARKS

Claims 30-34 are new; thus, claims 1-2, 4-9, 12-14, and 26-34 are all the claims pending in the application. Claims 1-2, 4-9, 12-14, and 26-29 stand rejected on prior art grounds. Applicants respectfully traverse the rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-2, 4-9, 12-14, and 26-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Luning (U.S. Patent No. 6,506,642) and Nandakumar (U.S. Patent No. 6,479,339). Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides an integrated circuit structure comprising first gate conductors, an oxide layer on the first gate conductors, and first spacers on the oxide layer. The structure further includes second gate conductors, the oxide layer on the second gate conductors, the first spacers on the oxide layer, an etch stop layer on the first spacers, and second spacers on the etch stop layer. In the rejection, the Office Action argues that the prior art of record disclose many features of the claimed invention. However, Luning and Nandakumar do not disclose an oxide layer on first and second gate conductors, wherein first spacers are on the oxide layer. Instead, the spacers of Luning are positioned directly on the gate conductors; Luning does not disclose an oxide layer on the gate conductors. Furthermore, Nandakumar discloses that a nitride film 270 (which the Office Action asserts teaches the "etch stop layer" of the claimed invention) is on the oxide layer 130; however, the nitride film 270 are not spacers. Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

Applicants traverse the rejections because the prior art of record fails to teach the claimed features of "an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer" (claims 26, 30, and 31).

More specifically, as illustrated in FIG. 8 of Applicants' disclosure, an oxide layer 106 is formed on an NFET gate conductor 102 and a PFET gate conductor 104. Moreover, first spacers 300 are formed on the oxide layer 106.

As illustrated in FIG. 3C of Nandakumar, an oxide film/layer 130 is formed on a gate conductor 110 and a gate conductor 120. However, Nandakumar does not disclose spacers on the oxide layer 130. Instead, a nitride film 270 (which the Office Action asserts teaches the "etch stop layer" of the claimed invention) is on the oxide layer 130.

Applicants submit that the nitride film 270 of Nandakumar do not teach the claimed "first spacers". More specifically, Applicants' claims define "an etch stop layer on said first spacers, and second spacers on said etch stop layer" (claims 1, 8, and 26).
Nandakumar does not disclose an etch stop layer on the nitride film 270 (which is on the oxide layer 130) and second spacers on the etch stop layer. Instead, Nandakumar only discloses a single layer of oxide film 280 on the nitride film 270.

In regards to Luning, Applicants submit that Luning fails to teach an oxide layer on the gate conductors 41 and 42 (FIG. 6). Instead, Luning discloses a sidewall spacer 60 on the gate conductor 41, and a sidewall spacer 44 on the gate conductor 42.

Accordingly, the prior art of record does not disclose an oxide layer on first and second gate conductors, wherein first spacers are on the oxide layer. Instead, the spacers of Luning are

positioned directly on the gate conductors; Luning does not disclose an oxide layer on the gate conductors. Furthermore, Nandakumar discloses that a nitride film 270 (which the Office Action asserts teaches the "etch stop layer" of the claimed invention) is on the oxide layer 130; however, the nitride film 270 are not spacers. Therefore, it is Applicants' position that the prior art of record fails to teach or suggest the claimed features of "an oxide layer, wherein said oxide layer is on said first gate conductors and said second gate conductors, and wherein said first spacers are on said oxide layer" as defined by claims 26, 30, and 31.

Therefore, it is Applicants' position that the prior art of record does not teach or suggest many features defined by independent claims 1, 8, 26 and that such claims are patentable over the prior art of record. Further, it is Applicants' position that dependent claims 2, 4-7, 9, 12-14, and 27-34 are similarly patentable, not only because of their dependency from a patentable independent claims, but also because of the additional features of the invention they defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-2, 4-9, 12-14, and 26-34, all the claims presently pending in the application, are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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